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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/716,947	11/18/2003	Jay T. Young	X-1386 US	6459

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EXAMINER	
DOAN, NGHIA M	

ART UNIT	PAPER NUMBER
2825	

DATE MAILED: 03/10/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/716,947	YOUNG ET AL.	
	Examiner	Art Unit	
	Nghia M. Doan	2825	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *03* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *18 November 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-6,11-17,22-28 and 33* is/are rejected.

7)☒ Claim(s) *7-10,18-21 and 29-32* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *18 November 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/18/2003*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. Responsive to communication application 10/716,947 filed on 11/18/2003. Claims 1-33 are pending in this Office Action.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1, 11-12, 22-23, and 33 are rejected under 35 U.S.C. 102(e) as being anticipated by Dante (US 6,907,592).

4. **With respect to claims 1, 12, and 23,** Dante teach a method (Dante, Abstract), computer instruction, and computer system (Dante, col. 9, 52-53) of routing a design in a programmable logic device (PLD) to increasing the effective of applying a multi-frame writer (MFW) technique (col. 3, ll. 23-55), comprising:

analyzing (determining) logic placement in the design (Dante, figure 5, col. 4, ll. 59-67, col. 5, ll. 1-12, and figure 9, steps 902 and 904, col. 7, ll. 42-46);

generating (building) a list of placement patterns including a list of nets associated with each placement pattern (routing table is built, routing table containing information such as the source and destination for each vector connection assembled,

which is placement patterns) (Dante, figure 5, col. 4, ll. 59-67, figure 7, col. 6, ll. 26-40, and figure 9, step 906, col. 7, ll. 45-47);

sorting list of placement (which is in table routing) the connections in descending order of cost parameters determined by a number of nets associated with each placement pattern (descending order from the higher cost parameter is less to used in routing a signal than the lower cost parameter) (Dante, figures 5-6, col. 5, ll. 13-36 and figure 9, step 908, col. 7, ll. 47-48); and

routing the nets associated with each placement pattern, in order from a placement pattern having a largest number of nets to a placement pattern having a smaller number of nets (descending order from the higher cost parameter is less to used in routing a signal than the lower cost parameter) (Dante, figures 5-6, col. 5, ll. 13-36, and col. 7, ll. 42-46).

5. **With respect to claims 11, 22, and 33,** Dante discloses all the limitation of claims are depended, and further limitation that wherein the PLD is a field programmable gate array (FPGA) (Dante, col. 3, ll. 21-25).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. **Claims 4-6, 11-12, 15-17, 22-23, 26-28, and 33 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adusumalli et al. (Adusumalli) (US 6,757,885) in view of Britton et al. (Britton) (US 5,394,031).**

8. **With respect to claims 4-6, 11-12, 15-17, 22-23, 26-28, and 33**, Adusumalli teaches a computer executed code, computer system (Adusumalli, col. 1, ll. 35-45), and method of routing a design (Adusumalli, col. 1, ll. 22-34), the method comprising: (**as claims 1, 12 and 23**) analyzing logic placement in the design (Adusumalli, fig. 1, step 104-108, col. 3, ll. 19-54); (**as claims 1, 12 and 23**) generating a list of placement patterns (connectivity matrix, tables I and II) as a result of analyzing the logic placement, the list of placement patterns (table II, PAIR column) including a list of nets (Table II, INTERCONNECTS) associated with each placement pattern (tables I and II) (Adusumalli, fig. 1, step 112, col. 3, ll. 58-62; and figure 3, col. 3, ll. 63-67 and col. 4, ll. 1-21); (**as claims 1, 12 and 23**) sorting the list of placement patterns in an order determined by a number of nets associated with each placement pattern (Adusumalli, figure 1, step 120, col. 4, ll. 30-38, Table II, PRIORITY associated with INTERCONNECTS); and (**as claims 1, 12 and 23**) routing the nets associated with each placement pattern, in order from a placement pattern having a largest number of nets to a placement pattern having a smaller number of nets (Adusumalli, fig. 1, step 120-122; and table II, example Priority (1) of pair (CU1/IOT) has 32 interconnections).

Adusumalli also at least suggest at figure 1, steps 106, 112 and 116, that user (designer) defines a hierarchical depth for generating connectivity matrix (placement pattern) of Compiler Unit (CU) and interconnect between CU and IO, that is based on

the decision step 112 and 116 to determined whether or not to complete routing design (**as claims 4-5, 15-16, and 26-27**) (Adusumalli, col. 3, ll. 28-50, ll. 58-62, and col. 4, ll. 24-26).

Adusumalli teaches a method and computer program performing routing for an VLSI integrated circuit as a function of the routing demand number and the routing resource number (Adusumalli, col. 2, ll. 43-45), but does not teach as a particular (**as claims 1, 12, and 23**) as performing routing for a programmable logic device (PLD) such as FPGA (**as claims 11, 22, and 33**) with using multi-frame write (MFW) technique for (**as claims 4-6, 15-17, and 26-28**) compressing a configuration bitstream of the routing resource for either fully routed design or does not fully routed design.

Britton does teach a method and apparatus for compressing data stream (bitstream) (Britton, col. 1, ll. 10-14) of using routing resource to perform routing (connecting) for (**as claims 11-12, 22-23, and 33**) a programmable logic device (PLD) such as FPGA) (Britton, col. 1, ll. 15-33) with using multi-frame write (MFW) technique in (**as claims 4-6, 15-17, and 26-28**) compressing a configuration bitstream (Britton, col. 5, ll. 46-68 and col. 6, ll. 1-3).

It would have been obvious to one of ordinary skill in the art at the time of invention can combine Adusumalli and Britton references to compress the configuration bitstream of the routing resource using the multi-frame technique that reducing the size of the bitstream for easily management and stored data (Britton, col. 1, ll. 55-63) and to configure (program) switches inside the FPGA to a desired state. These switches are controlling the configurable routing or logic on the FPGA (Britton, col. 1, ll. 26-33).

9. Claims 2-3, 13-14, and 24-25 are rejected under 35 U.S.C. 103(a) as being unpatentable over Adusumalli et al. (Adusumalli) (US 6,757,885) in view of Britton et al. (Britton) (US 5,394,031) and in further view of Putatunda et al. (Putatumda) (4,815,003).

10. **With respect to claims 2-3, 13-14, and 24-25**, Adusumalli and Britton teach all the limitation of claims are depended as the claim rejection 35 USC 103(a) above, but Adusumalli and Britton do not teach the further limitations of (**as claims 2, 13, and 24**) wherein the smaller number of nets is a predetermined threshold number and (**as claims 3, 14, and 25**) wherein the predetermined threshold number is four.

Putatumda does teach a method of optimizing for placement and routing of using a binary tree (Putatumda, figs. 8, 13, and 14a) for classifying from the highest order to lower order associated with placement configuration (Putatumda, col. 3, ll. 2-5). The binary tree structure is evaluated to identify as a subtrees (Putatumda, figs. 8, 13, and 14a) those structures in which the number of domains is less than a predetermined number placement configuration (predetermined threshold value) (Putatumda, col. 2, ll. 55-58, col. 6, ll. 4-31) and the predetermined number is four (fig. 14a, col. 14, ll. 63-68, col. 18, ll. 1-33).

It would have been obvious to one of ordinary skill in the art at the time of invention can combine Adusumalli, Britton, and Putatumda references for generating the predetermined threshold value for the placement configuration of using the binary tree and subtrees with the ideal placement configuration is four leaf nodes (col. 17, ll.

63-68) for simplifying and reducing time computation of generating placement configuration (col. 18, ll. 15-33).

Allowable Subject Matter

11. Claims 7-10, 18-21, and 29-32 are objected to as being dependent upon a rejected base claim, but would be allowable if the claims 7, 18 and 29 are rewritten in independent form including all of the limitations of the base claim and any intervening claims.

12. The following is a statement of reasons for the indication of allowable subject matter: (as claims 7, 18, and 29) the prior art of record does not teach or fairly suggest the further limitation of the method of routing a design in an PLD, wherein routing the nets associated with each placement pattern comprises for each placement pattern: selecting a plurality of sample nets from the list of nets associated with the placement pattern; generating a plurality of routing templates for each sample net and adding the routing templates to a cache of routing templates; selecting from the cache of routing templates a best template for unrouted nets associated with the placement pattern; and routing each unrouted net that can be routed using the best template.

Claims 8-10, 19-21, and 30-32 depend directly or indirectly on the claims 7, 18, and 29, respectively and there are also containing the allowable subject matter.

13. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Craft et al. (US 5,745,734) disclose a method of compressing configuration bit stream is receives a generalized data decompression engine which is used in configuration of the FPGA (Craft et al. col. 6, ll. 48-67); Scepanovic et al (US

5,838,585) disclose a method optimizing for placement and routing using the cost function associated with the wiring length.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Nghia M. Doan whose telephone number is 571-272-5973. The examiner can normally be reached on 8:30-5:30.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jack Chiang can be reached on 571-272-7483. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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